General Description

The AT2216 is a highly integrated, cost-effective approach for CobraNet® designs requiring 2 channels in and out. Using CobraNet® LE technology, it provides OEM product developers a smaller footprint and a significantly lower cost solution than a Cirrus Logic CS181002 or CS496102 CobraNet® 2-channel implementation.

In addition to CobraNet® audio networking and serial bridging features, CobraNet® LE technology also implements a number of features not available on a standard CobraNet® node. The AT2216 includes a serial host management interface (SHMI), 8 controllable GPIO pins, and access to eight 10-bit ADC channels.

Applications

- Powered loudspeakers
- CobraNet® audio endpoints
- Intercom stations
- Paging stations

Features

- Small overall footprint
- Low power suitable for use with Power over Ethernet (PoE)
- 2 x I2S digital audio inputs
- 2 x I2S digital audio outputs
- SHMI interface for local host control.
- 8 x GPIO pins individually set as inputs or outputs, and written/read via SHMI or via SNMP.
- 8 x 10-bit ADCs read via the SHMI, SNMP, or set to provide periodic updates via UDP packets.
- Serial bridging supported for transmission of control and metadata over the audio network

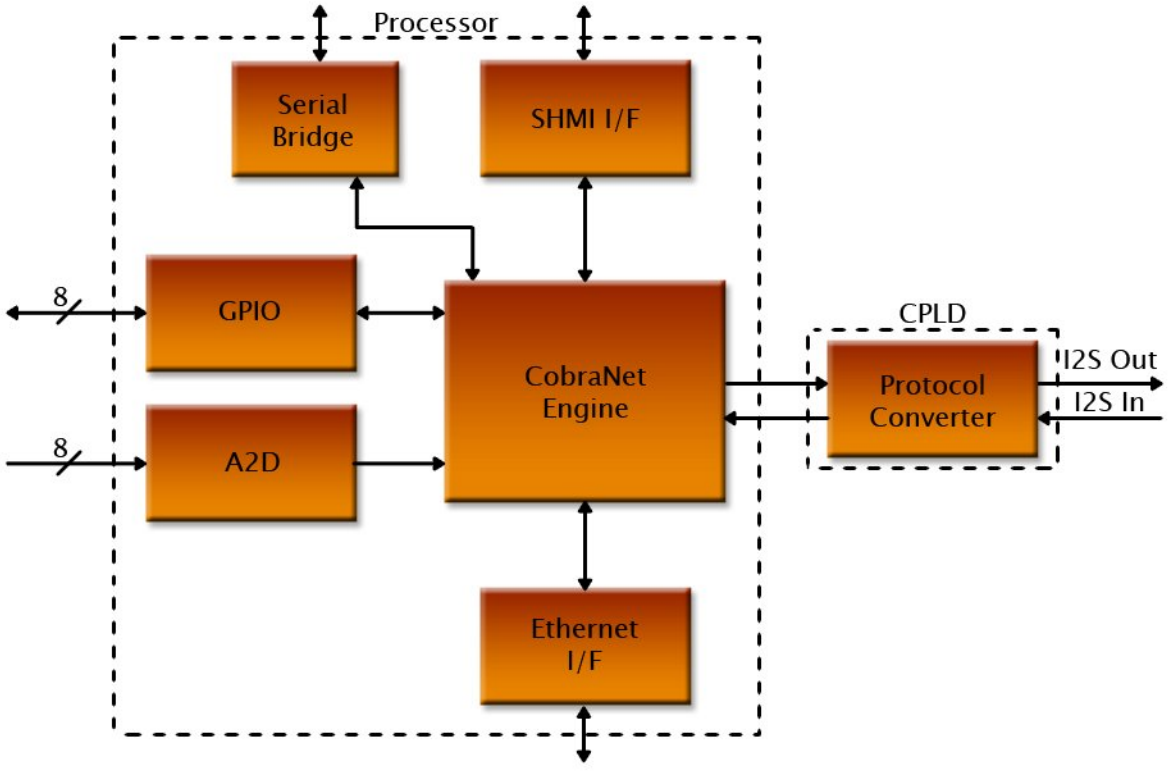

Figure 1 – Chipset Block Diagram

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Overview

The AT2216 chipset is comprised of 2 devices (see Figure 1). The main device is a processor that contains the CobraNet® Engine, an Ethernet interface, the serial interfaces for both the serial bridge and the serial hardware management interface (SHMI) as well as GPIO and ADC pins. The second device, a CPLD, contains the I2S digital audio interface.

NOTE: There are certain codecs that can be used in place of the CPLD but details of such a solution are beyond the scope of this document. For more details on using a codec, please contact Attero Tech directly.

Absolute Maximum Ratings

Processor

Parameter	Symbol	Min	Max	Unit
I/O supply voltage	VDD	0	4	V
Core supply voltage	VDD25	0	3	V
Analog supply voltage	VDDA	0	4	V
Ethernet PHY supply voltage	VCCPHY	0	4	V
Input voltage	VIN	-0.3	5	V
Maximum current per output pins	I	-	25	mA

CPLD

Parameter	Symbol	Condition	Min	Max	Unit
Supply Voltage	VCC	With respect to Ground	-0.5	4.6	V
DC input voltage	V_I		-2	5.75	V
DC output current, per pin	IOUT		-25	25	mA
Storage temperature		No bias	-65	150	˚C
Ambient temperature		Under bias	-65	135	˚C
Junction temperature		Under bias		135	˚C

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

Processor

Parameter	Parameter Name	Min	Nom	Max	Unit
VDD	I/O supply voltage	3.0	3.3	3.6	V
VDD25	Core supply voltage	2.25	2.5	2.75	V
VDDA	Analog supply voltage	3.0	3.3	3.6	V
VCCPHY	Ethernet PHY supply voltage	3.0	3.3	3.6	V
VIH	High-level input voltage	2.0	-	5.0	V
VIL	Low-level input voltage	-0.3	-	1.3	V
TA	Operating temperature range	-40	-	+85	˚C

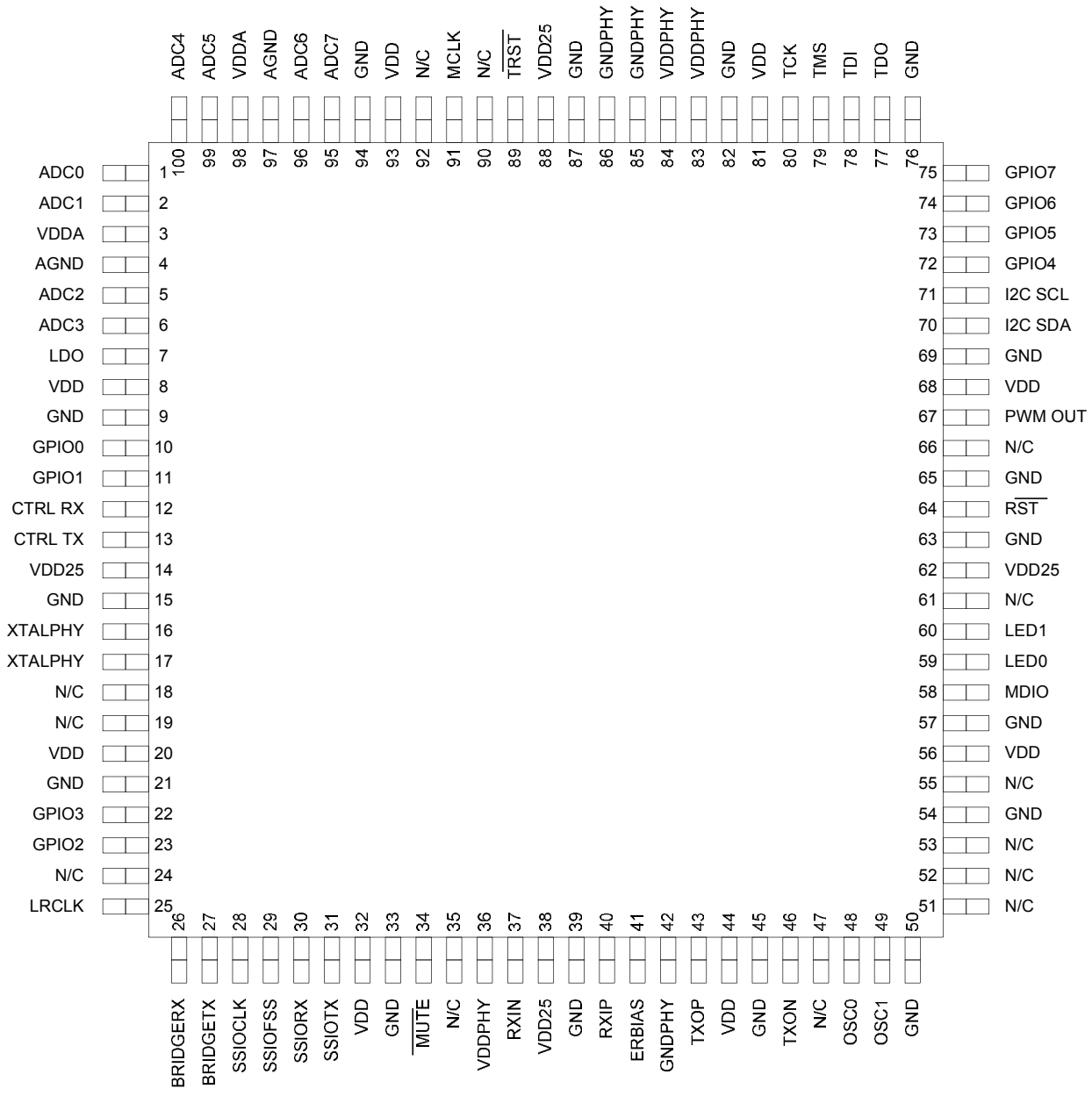
CPLD

Parameter	Parameter Name	Conditions	Min	Max	Unit
VCCINT	Supply voltage – internal logic and buffers	(1)	3.0	3.6	V
VCCIO	Supply voltage – output drivers (3.3V)		3.0	3.6	V
VCCISP	Supply Voltage – during ISP		3.0	3.6	V
VI	Input Voltage	(2)	-0.5	5.75	V
VO	Output Voltage		0	VCCIO	V
VIH	High level input voltage		1.7	5.75	V
VIL	Low-level input voltage		-0.5	0.8	V
VOH	High level output voltage		2.4		V
VOL	Low-level input voltage			0.4	V
TA	Ambient temperature		0	70	° C
TJ	Junction temperature		0	90	° C

(1) The POR time does not exceed 100 µs. The sufficient VCCINT voltage level for POR is 3.0 V. The device is fully initialized within the POR time after VCCINT reaches the sufficient POR voltage level.

(2) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before VCCINT and VCCIO are powered.

Processor Pin Out – 100-pin LQFP



Processor Signal Table

Pin number	Pin Name	Type	Description
1	ADC0	ANALOG	Analog-to-digital converter input 0.
2	ADC1	ANALOG	Analog-to-digital converter input 1.
3	VDDA	PWR	Positive supply for ADCs.
4	AGND	GND	Ground reference for the ADCs.
5	ADC2	ANALOG	Analog-to-digital converter input 2.
6	ADC3	ANALOG	Analog-to-digital converter input 3.
7	LDO	O	Low drop-out regulator output voltage.
8	VDD	PWR	Positive supply for I/O and logic.
9	GND	GND	GND reference for I/O and logic.
10	GPIO0	I/O	GPIO port bit 0.
11	GPIO1	I/O	GPIO port bit 1.
12	CTRL RX	I	SHMI receive port.
13	CTRL TX	O	SHMI transmit port.
14	VDD25	PWR	Positive supply for processor core and peripherals.
15	GND	GND	GND reference for I/O and logic.
16	XTALPHY	I	External crystal for Ethernet PHY.
17	XTALPHY	I	External crystal for Ethernet PHY.
18	N/C		
19	N/C		
20	VDD	PWR	Positive supply for I/O and logic.
21	GND	GND	GND reference for I/O and logic.
22	GPIO3	I/O	GPIO port bit 3.
23	GPIO2	I/O	GPIO port bit 2.
24	N/C		
25	LRCLK	O	48 kHz LRCLK input.
26	BRIDGERX	I	Serial Bridge receive line.
27	BRIDGETX	O	Serial Bridge transmit line.
28	SSIOCLK	O	SSI clock.
29	SSIOFSS	O	SSI frame.
30	SSIORX	I	SSI receive.
31	SSIOTX	O	SSI transmit.
32	VDD	PWR	Positive supply for I/O and logic.
33	GND	GND	GND reference for I/O and logic.
34	$\overline{\text{MUTE}}$	O	Audio mute output.
35	N/C		
36	VDDPHY	PWR	Positive supply Ethernet PHY.

37	RXIN	I	RXIN for Ethernet PHY.
38	VDD25	PWR	Positive supply for processor core and peripherals.
39	GND	GND	GND reference for I/O and logic.
40	RXIP	I	RXIP for Ethernet PHY.
41	GND	GND	GND reference for I/O and logic.
42	GND	GND	GND reference for I/O and logic.
43	TXOP	O	TXOP for Ethernet PHY.
44	VDD	PWR	Positive supply for I/O and logic.
45	GND	GND	GND reference for I/O and logic.
46	TXON	O	TXON for Ethernet PHY.
47	N/C		
48	OSC0	I	Processor oscillator pin.
49	OSC1	I	Processor oscillator pin.
50	GND	GND	GND reference for I/O and logic.
51	N/C		
52	N/C		
53	N/C		
54	GND	GND	GND reference for I/O and logic.
55	N/C		
56	VDD	PWR	Positive supply for I/O and logic.
57	GND	GND	GND reference for I/O and logic.
58	MDIO	I/O	MDIO of the Ethernet PHY.
59	LEDY	O	LED drive output for LH Ethernet LED.
60	LEDG	O	LED drive output for RH Ethernet LED.
61	N/C		
62	VDD25	PWR	Positive supply for processor core and peripherals.
63	GND	GND	GND reference for I/O and logic.
64	$\overline{\text{RST}}$	I	System reset pin.
65	GND	GND	GND reference for I/O and logic.
66	N/C		Factory use only.
67	PWM1	O	PWM control for external VXCO.
68	VDD	PWR	Positive supply for I/O and logic.
69	GND	GND	GND reference for I/O and logic.
70	I2C SCL	O	I^2C clock output.
71	I2C SDA	I/O	I^2C data.
72	GPIO4	I/O	GPIO port bit 4.
73	GPIO5	I/O	GPIO port bit 5.
74	GPIO6	I/O	GPIO port bit 6.

75	GPIO7	I/O	GPIO port bit 7.
76	GND	GND	GND reference for I/O and logic.
77	TDO	O	JTAG TDO.
78	TDI	I	JTAG TDI.
79	TMS	I	JTAG TDS.
80	TCK	I	JTAG CLK.
81	VDD	PWR	Positive supply for I/O and logic.
82	GND	GND	GND reference for I/O and logic.
83	VDDPHY	PWR	Positive supply for Ethernet PHY.
84	VDDPHY	PWR	Positive supply for Ethernet PHY.
85	GND	GND	GND reference for I/O and logic.
86	GND	GND	GND reference for I/O and logic.
87	GND	GND	GND reference for I/O and logic.
88	VDD25	PWR	Positive supply for processor core and peripherals.
89	$\overline{\text{TRST}}$	I	JTAG reset.
90	N/C		
91	MCLK CNTL	O	MCLK control output.
92	N/C		
93	VDD	PWR	Positive supply for I/O and logic.
94	GND	GND	GND reference for I/O and logic.
95	ADC7	ANALOG	Analog-to-digital converter input 7.
96	ADC6	ANALOG	Analog-to-digital converter input 6.
97	AGND	GND	Ground reference for the ADCs.
98	VDDA	PWR	Positive supply for the ADCs.
99	ADC5	ANALOG	Analog-to-digital converter input 5.
100	ADC4	ANALOG	Analog-to-digital converter input 4.

Power

Two different supplies are required by the AT2216 processor. The main voltage is 3.3V (VDD, VDDA & VDDPHY). This should be used for the majority of the power supplies on both chipset devices though additional filtering may be required particularly for the analog power pins VDDA on the processor. The processor also requires a 2.5V supply for its internal logic. However, the processor provides an integrated LDO regulator that may be used to provide this supply. The +2.5V is thus available at the LDO pin. If this is used, it should be connected to all the VDD25 pins on the processor with an external bulk capacitor > 1 uF, to ground.

It is recommended that all the power pins be decoupled to ground with a 0.1 uF capacitor as close to each pin as possible.

Clocking

The processor requires two external crystals. The OSC0 and OSC1 inputs use an 8.0 MHz crystal and the XTALPHY inputs require a 25.0 MHz crystal.

An additional 24.576 MHz VXCO is also required for the AT2216 to generate the master clock. Voltage control is provided by the processors PWM output, PWM1 which is passed through an RC filter to obtain a steady DC level. The reference design uses a Joyous ZYCA5A1-24.576M.

SSI Interface

The audio streams are passed between the processor and CPLD as an SSI stream of data. The CPLD converts the SSI into I2S format to allow it to be used with standard ADCs and DACs. The interface consists of 4 signals: SSIOTX, SSIORX, SSIOFDD and SSIOCLK. Note there are two additional signals that link the processor and the CPLD. These are the LRCLK input and the MCLK CTRL output pins. The LRCLK is required by the processor to correctly encode and/or decode the audio signals on the SSI bus. The MCLK CTRL pin is used to control the MCLK signal.

NOTE: While the AT2216 chipset supports transmission and reception of 16-, 20-, and 24-bit CobraNet audio data, a hardware limitation means that the data sent and received over the SSI bus restricts the data width to 16-bits only. Audio data with more than 16-bits being transferred to the DAC is truncated. Audio data received from the ADC is shifted and padded as required.

ADC Inputs

The AT2216 chipset has eight ADC inputs which can be set up to measure any analog signals. The values can be read via the SNMP, or the SHMI interface. Since the AT2216 chipset does not in itself support metering, the ADCs could be used to meter the incoming or outgoing analog audio signals. The ADC inputs may also be used to monitor system variables. For example, in a CobraNet-enabled power amplifier, the ADC inputs could be used to monitor temperature, output current, and output voltage.

GPIO Pins

The AT2216 chipset has eight GPIO pins. These are configured via SNMP or the SHMI. Each pin can be set individually as either an output or an input. They can be set or read via SNMP or SHMI.

I²C Interface

The processor requires 64 kBits of external non-volatile memory in order to provide persistence of variables during power down. Two pins are provided for the I2C bus, I2C SCL, and I2C SDA. The reference design uses a Microchip Tech 24LC64-I/SN.

Ethernet Interface

The main parts of the Ethernet PHY are contained with the AT2216 IC itself. There are four data lines, RXIP, RXIN, TXOP, and TXON. There is also an MDIO control pin as well as two LED status pins, LED0 and LED1. The MDIO pin must be connected through a 10k Ω pull-up resistor to the +3.3 V supply. The LED signals indicate the various states of operation of the Ethernet Controller. The low power requirement of the AT2216 also means that Power over Ethernet (PoE) can also be supported.

Serial Bridge Interface

CobraNet® also has a serial bridge feature which allows devices connected on a CobraNet® network to send serial data to one another. There are 2 pins available for this purpose, BRIDGERX and BRIDGETX. Both signals use 3.3V logic levels but are 5V tolerant. The format and baud rate are set within the CobraNet® device itself.

SHMI Port Interfacing

The AT2216 will receive messages from any source capable of communicating serially using 8 data bits, no parity bit, 1 stop bit, and no flow control with a default baud rate of 57600 bits per second (bps). The baud rate is configurable but the data bits, stop bits, flow control, and parity are not. The baud rate may be set to 9600, 19200, 38400, 57600, or 115200 bits per second. The SHMI uses CTRL RX for receiving data and CTRL TX for transmitting data.

For details on how to change the baud rate as well as all the details on how to control all the various CobraNet® aspects of the module, see the CobraNet® LE Software API.

Other Signals

The $\overline{\text{RST}}$ pin is the system reset and is negative true. This should be held low on power up while PSU voltages are stabilized. It can be tied to the CPLD's $\overline{\text{RST}}$ pin. The $\overline{\text{MUTE}}$ signal is used to mute the outputs. This is active on power up or reset until the device has initiated and prevents unwanted audio being output during initialization. It is also active whenever a loss of sync happens, beat packets are lost, or audio packets go missing,

Power Specifications

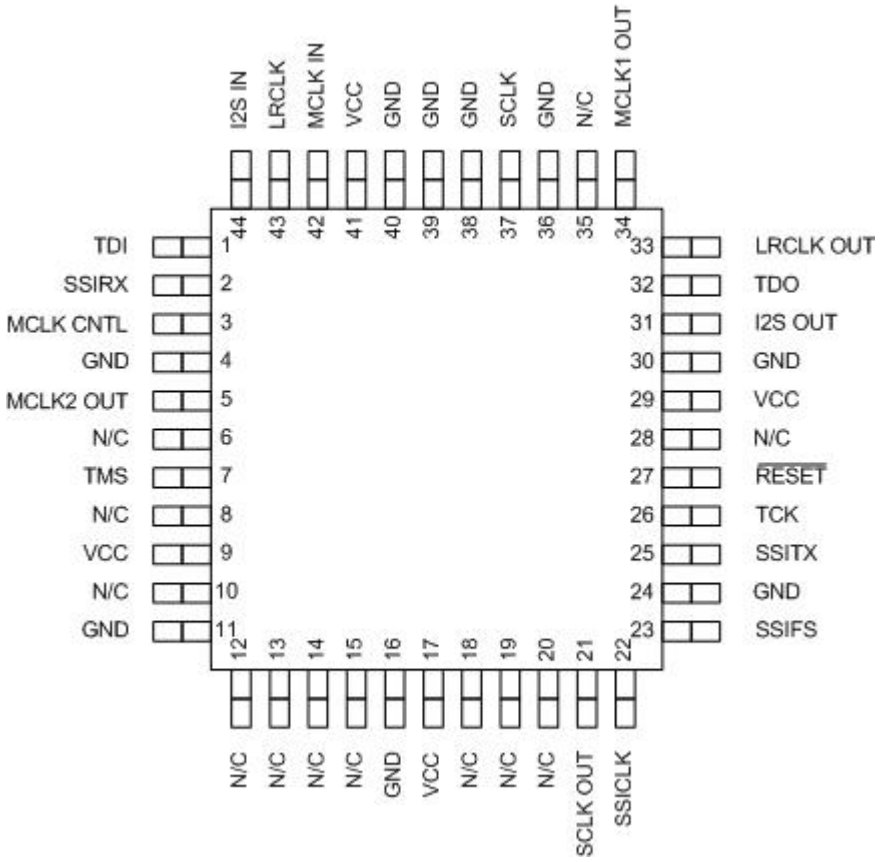
The power measurements specified in the tables that follow are run on the core processor using SRAM with the following specifications (except as noted):

- VDD = 3.3 V
- VDD25 = 2.50 V
- VDDA = 3.3 V
- VDDPHY = 3.3 V
- Temperature = 25˚C
- Clock Source (MOSC) =3.579545 MHz Crystal Oscillator
- Main oscillator (MOSC) = enabled
- Internal oscillator (IOSC) = disabled

Parameter	Parameter Name	Conditions	3.3 V V_{DD}, V_{DDA}, V_{DDPHY}		2.5 V V_{DD25}		Unit
			Nom	Max	Nom	Max	
IDD_RUN	Run mode 1 (Flash loop)	VDD25 = 2.50 V Code= while(1){} executed in Flash Peripherals = All ON System Clock = 50 MHz (with PLL)	48	n/a	108	n/a	mA
	Run mode 2 (Flash loop)	VDD25 = 2.50 V Code= while(1){} executed in Flash Peripherals = All OFF System Clock = 50 MHz (with PLL)	5	n/a	52	n/a	mA
	Run mode 1 (SRAM loop)	VDD25 = 2.50 V Code= while(1){} executed in SRAM Peripherals = All ON System Clock = 50 MHz (with PLL)	48	n/a	100	n/a	mA
	Run mode 2 (SRAM loop)	VDD25 = 2.50 V Code= while(1){} executed in SRAM Peripherals = All OFF System Clock = 50 MHz (with PLL)	5	n/a	45	n/a	mA

CPLD Pin Out – 44-pin TQFP

The CPLD is an Altera EPM3032ATC44-10N.



CPLD Signal Table

Pin Number	Pin Name	Type	Description
1	TDI	I	JTAG TDI.
2	SSIRX	I	SSI receive.
3	MCLK CNTL	I	MCLK source control.
4	GND	GND	GND reference for I/O and logic.
5	MCLK2 OUT	O	I2S MCLK for audio outputs.
6	N/C		
7	TMS	I/O	JTAG TMS.
8	N/C		
9	VCC	PWR	Positive supply for I/O and logic.
10	N/C		
11	GND	GND	GND reference for I/O and logic.
12	N/C		
13	N/C		
14	N/C		

15	N/C		
16	GND	GND	GND reference for I/O and logic.
17	VCC	PWR	Positive supply for I/O and logic.
18	N/C		
19	N/C		
20	N/C		
21	SCLK OUT	O	I2S SLCK for audio outputs.
22	SSICLK	I	SSI clock.
23	SSIFS	I	SSI frame.
24	GND	GND	GND reference for I/O and logic.
25	SSITX	O	SSI transmit.
26	TCK	I	JTAG TCK.
27	$\overline{\text{RESET}}$	I	System reset pin.
28	N/C		
29	VCC	PWR	Positive supply for I/O and logic.
30	GND	GND	GND reference for I/O and logic.
31	I2S OUT	O	I2S digital audio output data.
32	TDO	O	JTAG TDO.
33	LRCLK OUT	O	I2S LRCLK for audio outputs.
34	MCLK1 OUT	O	I2S MCLK signal for audio inputs.
35	N/C		
36	GND	GND	GND reference for I/O and logic.
37	SCLK	O	I2S SCLK for audio inputs.
38	GND	GND	GND reference for I/O and logic.
39	GND	GND	GND reference for I/O and logic.
40	GND	GND	GND reference for I/O and logic.
41	VCC	PWR	Positive supply for I/O and logic.
42	MCLK IN	I	MCLK input from VXCO.
43	LRCLK	O	I2S LRCLK for audio inputs.
44	I2S IN	I	I2S digital audio input data.

NOTE: Attero Tech does not supply the CPLD. However, users of the AT2216 will be supplied with the firmware binary file to program the CPLD for no charge.

I²S Audio Timing Diagrams

There is a single synchronous serial input and a single serial output interface coming from the CPLD. Each interface contains two channels of audio in one sample period of the LRCLK audio word clock. The following diagram shows the timing characteristics.

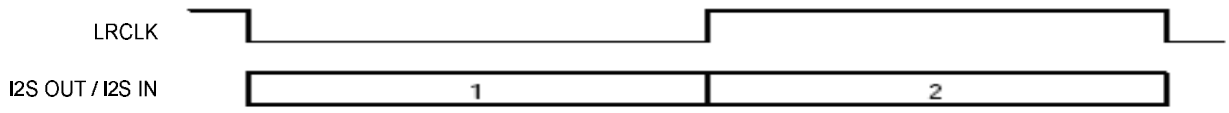


Figure 2 - Channel Structure for Synchronous Serial Audio (One Sample Period)

Default channel ordering is shown above. Note that the first channel always begins after the falling edge of LRCLK. SCLK period depends on the sample rate selected. Up to 32 significant bits are received and buffered by the module for synchronous inputs. Up to 32 significant bits are transmitted by the module for synchronous outputs. Bit 31 is always the most significant (sign) bit. A 16-bit audio source must drive to bit periods 31-16 with audio data and bits 15-0 should be actively driven with either a dither signal or zeros. Cirrus Logic recommends driving unused LS bits to zero. Although data is always transmitted and received with a 32-bit resolution by the synchronous serial ports, the resolution of the data transferred to/from the Ethernet may be less. Incoming audio data is truncated to the selected resolution. The unused least significant bits on outgoing data are zero filled.

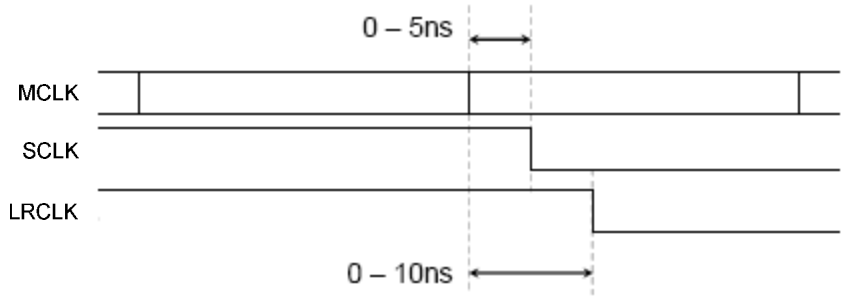


Figure 3 - Timing Relationship Between MCLK, SCLK and LRCLK

An SCLK edge follows an MCLK2 edge by 0.0 to 5.0ns. An LRCLK edge follows a MCLK2 edge by 0.0 to 10.0ns.

Note: The SCLK and LRCLK might be synchronized with the either the falling edge or the rising edge of MCLK. Which edge is impossible to predict since it depends on power up timing.

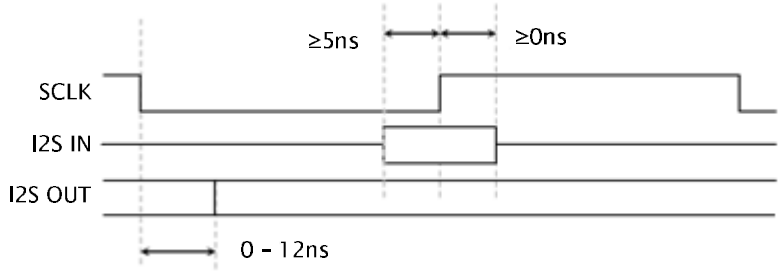


Figure 4 - Serial Port Data Timing Overview

Setup times for I2S IN and LRCLK are 5.0 ns with a hold time of 0.0 ns with respect to the SCLK edge. Clock to output times for I2S OUT is 0.0 to 12.0 ns from the edge of SCLK.

I²S Data Timing

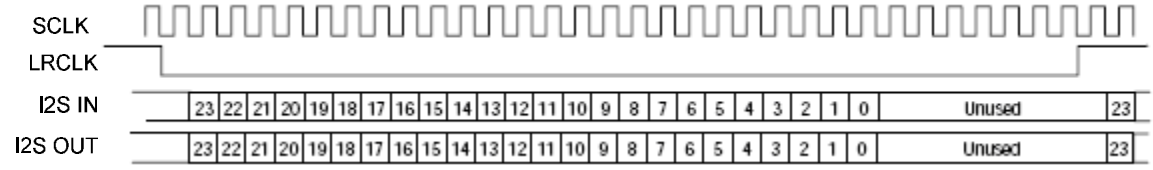


Figure 5 - Audio Data Timing Detail - I2S Mode, 64FS

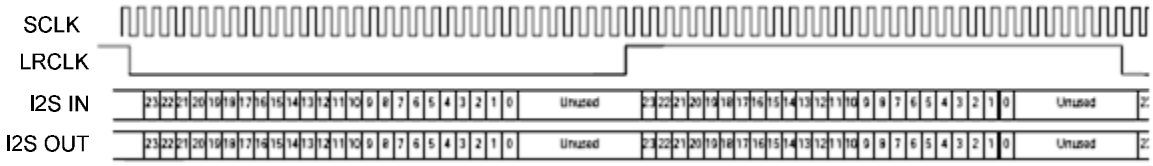


Figure 6 - Audio Data Timing Detail - I2S Mode, 128FS

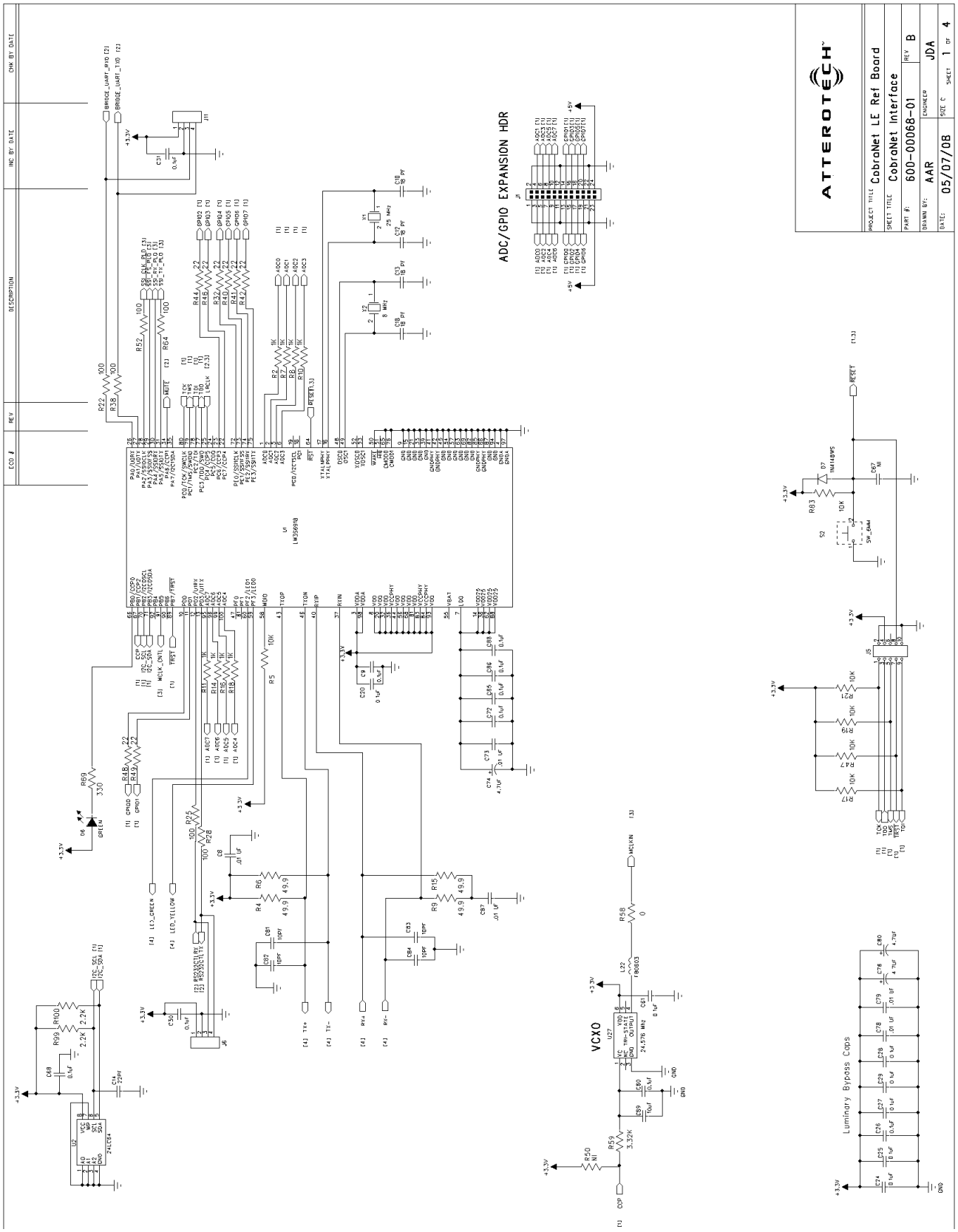
Each audio channel is comprised of 32 bits of data, regardless of audio sample size. The figure above shows 24-bit audio data. The MSB is left justified and arrives one bit period following LRCLK. Data is sampled on the rising edge of SCLK and data changes on the falling edge.

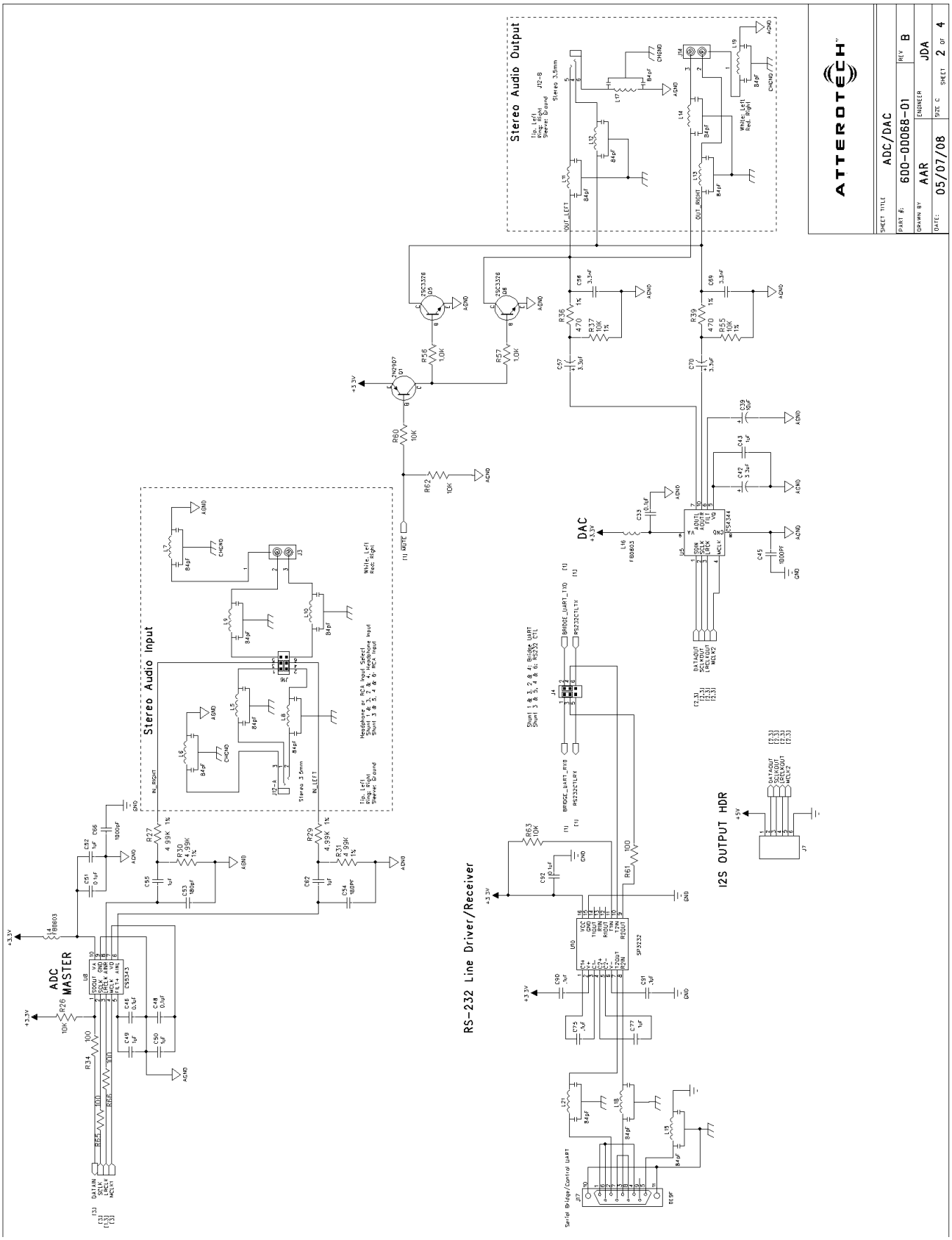
Reference Design

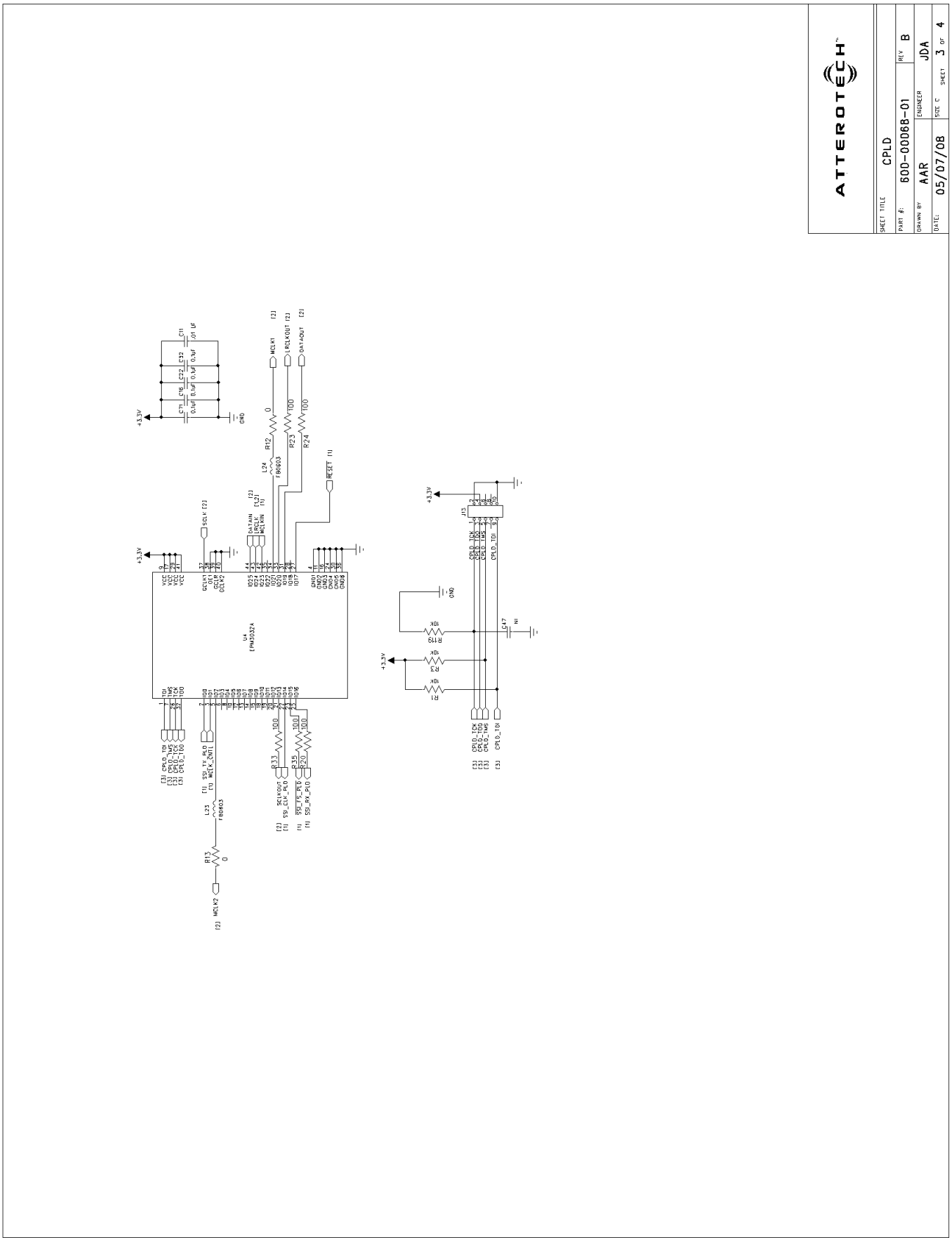
The following schematics from the reference design board have been included as an example of how to connect the AT2216 chipset. The reference design shows how to correctly connect the processor and CPLD together and marry them up to the external components such as ADCs and DACs.

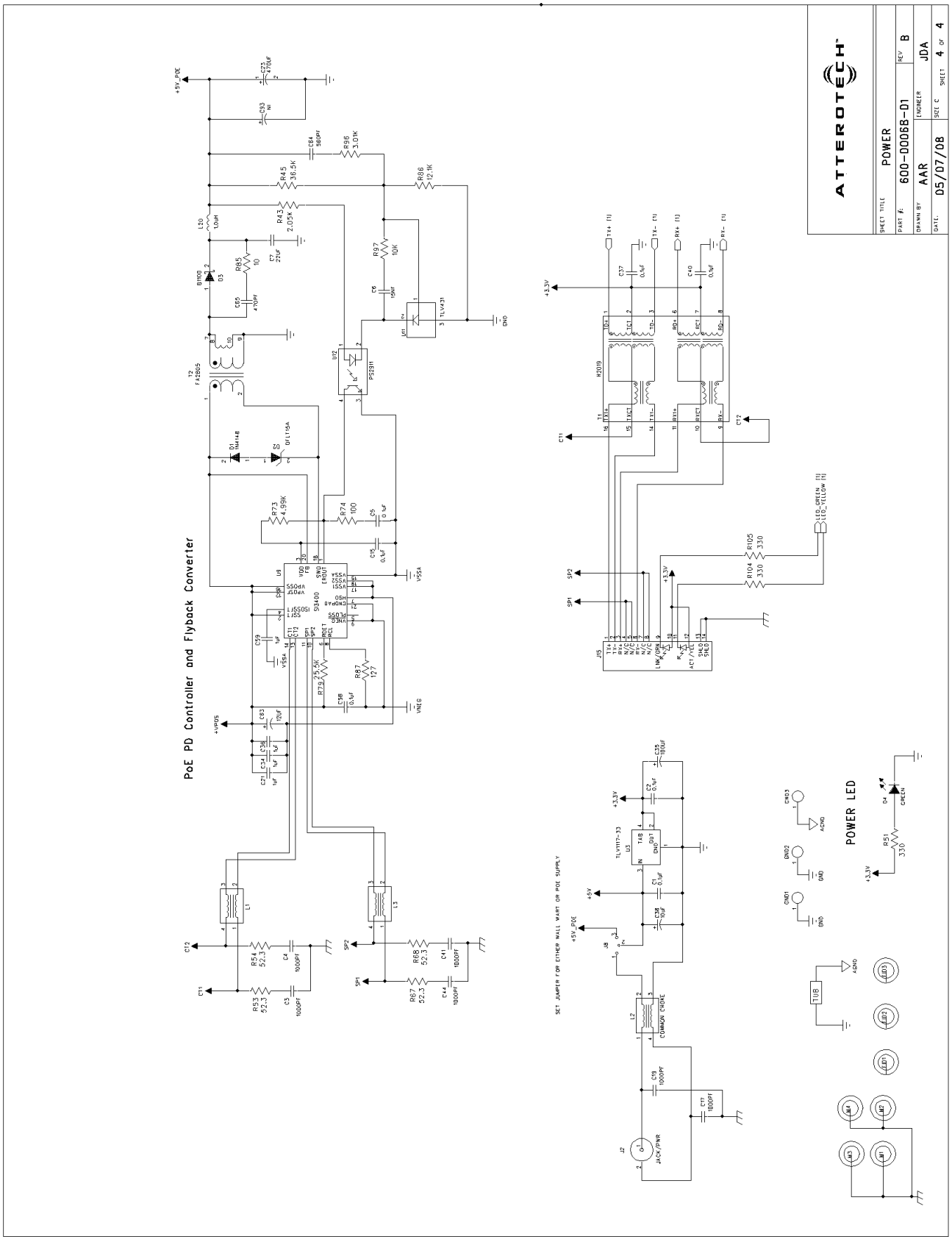
The reference design example has 2 single-ended outputs and 2 single-ended inputs each with a choice of RCA or 1/8" mini-jack connectors. It also includes an 802.3af compliant PoE power supply. More details on the reference design are available in the AT2216 Reference Design datasheet.

Note: Many of the headers and jumpers included in the reference design are to allow configuration or testing with customers own external circuitry. Production designs need not include these connectors. These include J1, J4, J5, J6, J7, J8, J11, J13, J16, and J17.


ADC/GPIO EXPANSION HDR
VCXO
Luminary Bypass Caps
ATTEROTECH
PROJECT TITLE CobraNet LE Ref Board
SHEET TITLE CobraNet Interface
PART #: 600-00068-01
REV B
DRAWN BY: AAR
ENGINEER JDA
DATE: 05/07/08
SIZE C
SHEET 1 OF 4


Stereo Audio Output
Stereo Audio Input
DAC
ADC MASTER
RS-232 Line Driver/Receiver
I2S OUTPUT HDR
ATTEROTECH
SHEET TITLE ADC/DAC
PART #: 600-00068-01 REV B
DRAWN BY AAR ENGINEER JDA
DATE: 05/07/08 SIZE C SHEET 2 OF 4


ATTEROTECH
SHEET TITLE CPLD
PART #: 600-00068-01 REV B
DRAWN BY AAR ENGINEER JDA
DATE: 05/07/08 SIZE C SHEET 3 OF 4


PoE PD Controller and Flyback Converter
POWER LED
SET JUMPER FOR EITHER WALL WART OR POE SUPPLY
ATTEROTECH
SHEET TITLE POWER
PART #: 600-00068-01 REV B
DRAWN BY AAR ENGINEER JDA
DATE: 05/07/08 SIZE C SHEET 4 OF 4

Ordering Information

Part Number	Description
AT2216	AT2216 CobraNet LE Processor
900-00111-01	AT2216 Reference Design Evaluation Board

NOTE: Attero Tech does not supply the CPLD support device. However, users of the AT2216 will be supplied with the firmware binary file to program the CPLD for no charge.