

General Description

The CDK-8 is a low cost CobraNet® interface module that provides OEM product developers a simple and cost effective means of adding CobraNet® audio networking capability to their products. The CDK-8 supports 8 bi-directional audio transport and has a user configurable DSP for audio processing. In addition to a basic CobraNet® module, Attero Tech also offers modules with a Host Management Interface (HMI) port connector or with a Serial Host Management Interface Port (SHMI).

Applications

- Powered loudspeakers
- Multi-channel paging systems
- Security systems
- Two-channel and multi-channel power amplifiers
- Residential multi-zone audio networking

Features

- 100BASE-Tx, 100 Mbps, full duplex Ethernet, fully compliant with IEEE 802.3u
- Support for 48/96kHz sampling rates at up to 24 bits
- Serial bridging supported for transmission of control and metadata over the audio network
- High quality, low jitter clock source
- SNMP agent for control, monitoring, and remote management
- TFTP support for firmware updates over the network
- Can be powered through the RJ-45 jack (external regulation required)
- Status LEDs for CobraNet® conductor and CobraNet® activity as well as error reporting
- Compact 3"x3" form factor (3"x3.5" w/HMI or UART HMI support)
- All logic levels are 3.3V and signal inputs are 5V tolerant.

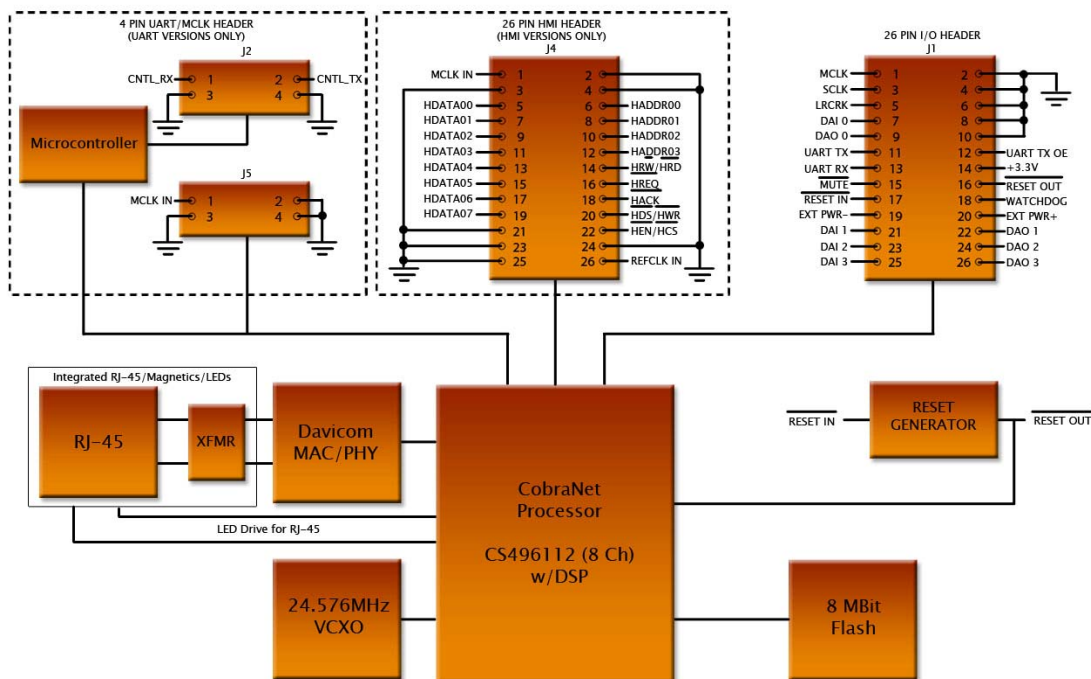


Figure 1 - Block Diagram

CobraNet® is a trademark of Cirrus Logic, Inc

Overview

The CDK module comes in 3 forms all based around the same hardware and utilizing the same footprint. The CDK-8D is the base model. Powered from 3.3 V, it is a complete CobraNet® node with 8 digital audio inputs¹ and 8 digital audio outputs², an Ethernet connection, and a user configurable DSP. Device control is accomplished via SNMP through the Ethernet connection.

For embedded local control, there is the CDK-8DHMI. In addition to the features of the CDK-8D, the CDK-8DHMI includes the HMI port. The HMI port allows a microprocessor or microcontroller to read and modify parameters within the CobraNet® node locally without having to use SNMP over the network connection.

The final device in the family is the CDK-8DUART. This device retains all the functionality of the CDK-8DHMI but replaces the parallel HMI port with a standard serial connection making the interface easier to implement and requiring less interface pins on the host microcontroller. Using a serial protocol, a microcontroller can then communicate with the CobraNet® node, achieving the same control as available with the CDK-8DHMI.

Recommended Operating Conditions

Parameter	Symbol	Nominal
DC supply	V	3.3 V
Input Current	I _{in}	600 mA
Temperature (Ambient)	T _A max	40 °C

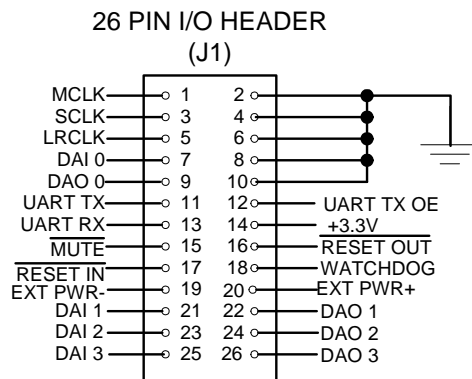
¹ There are 4 digital input pins but each support 2 channels giving 8 input channels in total.

² There are 4 digital output pins but each support 2 channels giving 8 output channels in total.

Digital Audio Interfacing

Access to the audio signals and clocks as well as various control signals on all three devices is via a 26-way 0.1" female header. This header, J1, has the same pin-out on all three devices and is in the same physical location.

Pin Descriptions for J1



Pin	Signal	Direction	Notes
14	+3.3V	PWR	+3.3V power input
2,4,6,8,10	GND	GND	GND
19	EXT PWR-	OUT	Connected to unused pair on Ethernet RJ-45 connector. Can be used to remotely power device connected to header. (Negative)
20	EXT PWR+	OUT	Connected to unused pair on Ethernet RJ-45 connector. Can be used to remotely power device connected to header. (Positive)
15	$\overline{\text{MUTE}}$	OUT	Active low during initialization and when faults are detected
16	$\overline{\text{RESET OUT}}$	OUT	Active low reset signal generated by the CDK-8 module
17	$\overline{\text{RESET IN}}$	IN	Active low reset signal generated by external circuitry
18	WATCHDOG	OUT	Toggles at 750 Hz indicating proper operation. If the period exceeds 200ms, this indicates hardware or software malfunction and the module needs to be reset.
1	MCLK	OUT	24.576 MHz Master Audio Clock
3	SCLK	OUT	Serial Audio Bit Clock (64 FS)
5	LRCLK	OUT	Audio Word Clock (FS)
7	DAI 0	IN	I2S Synchronous Serial Audio Data Input CDK-8 = Channels 1 & 2
21	DAI 1	IN	I2S Synchronous Serial Audio Data Input CDK-8 = Channels 3 & 4

23	DAI 2	IN	I2S Synchronous Serial Audio Data Input CDK-8 = Channels 5 & 6
25	DAI 3	IN	I2S Synchronous Serial Audio Data Input CDK-8 = Channels 7 & 8
9	DAO 0	OUT	I2S Synchronous Serial Audio Data Output CDK-8 - Channels 1 & 2
22	DAO 1	OUT	I2S Synchronous Serial Audio Data Output CDK-8 = Channels 3 & 4
24	DAO 2	OUT	I2S Synchronous Serial Audio Data Output CDK-8 = Channels 5 & 6
26	DAO 3	OUT	I2S Synchronous Serial Audio Data Output CDK-8 = Channels 7 & 8
11	UART TX	OUT	Serial bridge asynchronous serial transmit data line. Transmits data received by this node from other CobraNet® devices on the CobraNet® network.
12	UART TX OE	OUT	Serial bridge asynchronous serial transmit output enable
13	UART RX	IN	Serial bridge asynchronous serial receive data line. Receives data that will be transmitted across the CobraNet® network to other CobraNet® devices. Pull up to 5V if not used.

The format of the synchronous serial audio interface can be changed with customized firmware. The formats supported are I2S, Cirrus Standard Mode and Normal Mode.

Power Requirements

The CDK-8 requires a regulated +3.3 VDC supply at 600 mA and power consumption is approximately 2 W. Since the EXT PWR connections are connected to the unused pairs on the Ethernet cable, they do not power the unit directly but can be used to power the module from a remote source. It is recommended that the incoming external power be regulated locally before being supplied to the module.

Clocking Notes

All CDK-8 modules generate their own master clock but the HMI and UART versions of the module also have the facility to synchronize with an external master audio clock through the MCLK_IN pin. However, in order to do so, a firmware change will be required. Contact ProductSupport@atterotech.com for more details.

It should be noted that the MCLK output signal (J1 - Pin 1) is generated from the VCXO on the CDK-8 module and thus will differ from the MCLK_IN clock signal. As a result, if an external MCLK is used, all components (ADCs, DACs, etc.) on the target hardware that are driven by the master clock should use the same clock supplied to the MCLK_IN pin of the CDK-8 module and not the MCLK output from the module.

Digital Audio Timing Diagrams

There are four synchronous serial input and output interfaces coming from the CDK module. Each interface contains two channels in one sample period of the LRCLK audio word clock. The following diagram shows the timing characteristics. The characteristics are the same at both 48 kHz and 96 kHz sample rates. The CDK-8 supports all four serial interfaces.

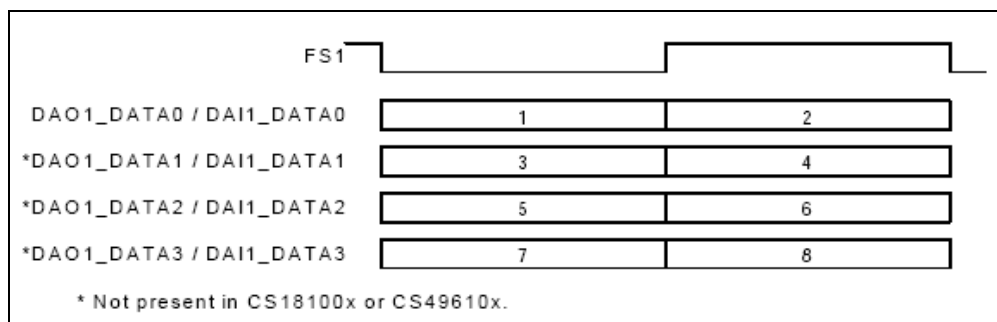


Figure 2 - Channel Structure for Synchronous Serial Audio at 64FS (One Sample Period)

Default channel ordering is shown above. Note that the first channel always begins after the rising or falling edge of FS1 (depending on the mode). DAI1_SCLK period depends on the sample rate selected. Up to 32 significant bits are received and buffered by the module for synchronous inputs. Up to 32 significant bits are transmitted by the module for synchronous outputs. Bit 31 is always the most significant (sign) bit. A 16-bit audio source must drive to bit periods 31-16 with audio data and bits 15-0 should be actively driven with either a dither signal or zeros. Cirrus Logic recommends driving unused LS bits to zero. Although data is always transmitted and received with a 32-bit resolution by the synchronous serial ports, the resolution of the data transferred to/from the Ethernet may be less. Incoming audio data is truncated to the selected resolution. The unused least significant bits on outgoing data is zero filled.

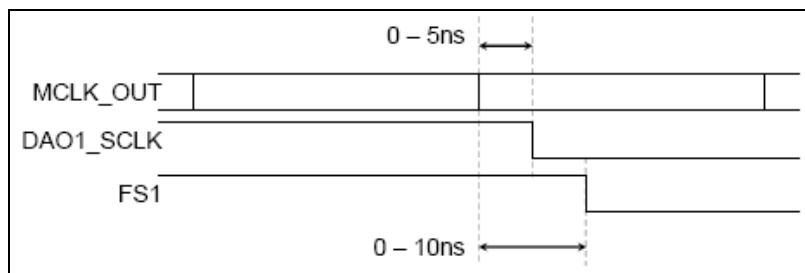


Figure 3 - Timing Relationship between FS512_OUT, DAO1_SCLK and FS1

A DAO1_SCLK edge follows an MCLK_OUT edge by 0.0 to 5.0 ns. An FS1 edge follows a MCLK_OUT edge by 0.0 to 10.0 ns.

Note: The DAO1_SCLK and FS1 might be synchronized with either the falling edge or the rising edge of MCLK_OUT. Which edge is impossible to predict since it depends on power up timing.

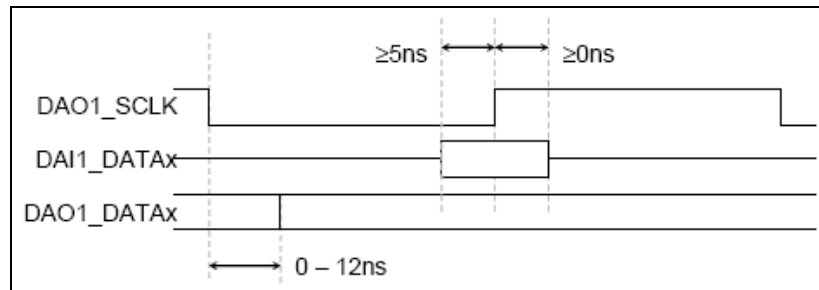


Figure 4 - Serial Port Data Timing Overview

Setup times for DAI1_DATAx and FS1 are 5.0 ns with a hold time of 0.0 ns with respect to the DAI1_SCLK edge. Clock to output times for DAO1_DATAx is 0.0 to 12.0 ns from the edge of DAO1_SCLK.

Normal Mode Data Timing

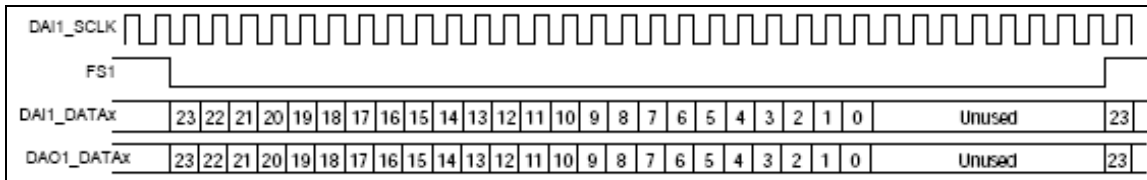


Figure 5 - Audio Data Timing Detail - Normal Mode, 64FS

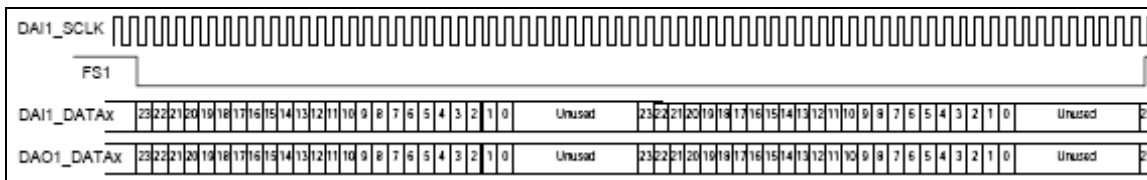


Figure 6 - Audio Data Timing Detail - Normal Mode, 128FS

Each audio channel is comprised of 32 bits of data, regardless of audio sample size. The figure above shows 24-bit audio data. The MSB is left justified and is aligned with FS1. Data is sampled on the rising edge of DAI_SCLK and data changes on the falling edge.

I2S Mode Data Timing

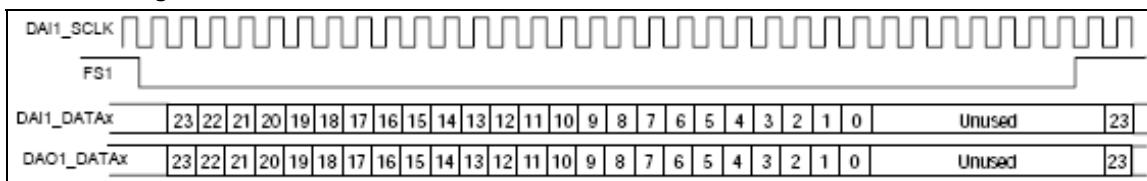


Figure 7 - Audio Data Timing Detail - I2S Mode, 64FS

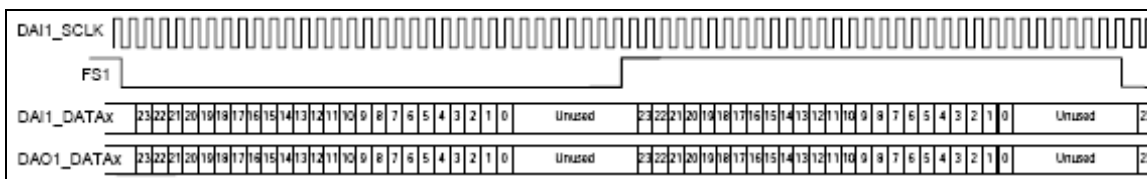


Figure 8 - Audio Data Timing Detail - I2S Mode, 128FS

Each audio channel is comprised of 32 bits of data, regardless of audio sample size. Figure 8 shows 24-bit audio data. The MSB is left justified and arrives one bit period following FS1. Data is sampled on the rising edge of DAI_SCLK and data changes on the falling edge.

Standard Mode Data Timing

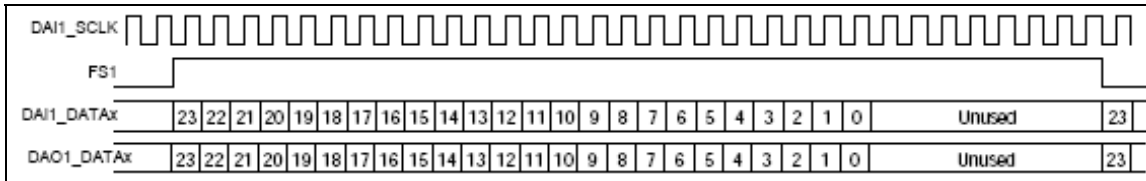


Figure 9 - Audio Data Timing Detail - Standard Mode, 64FS

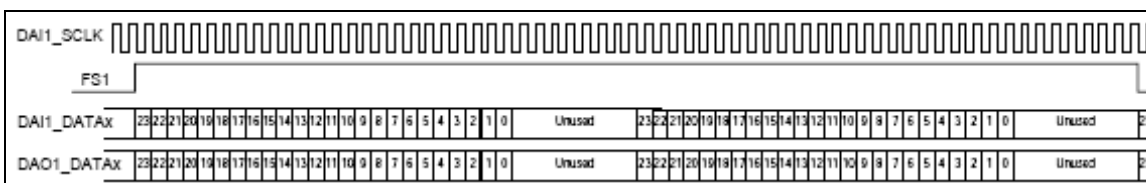


Figure 10 - Audio Data Timing Detail - Standard Mode, 128FS

Each audio channel is comprised of 32 bits of data, regardless of audio sample size. The figure above shows 24-bit audio data. The MSB is left justified and is aligned with FS1. Data is sampled on the rising edge of DAI_SCLK and data changes on the falling edge.

Serial Bridge Interface

CobraNet® also has a serial bridge feature which allows devices connected on a CobraNet® network to send serial data to one another. There are three pins available for this purpose. All the signals use 3.3 V logic levels but are 5 V tolerant. The format and baud rate are set within the CobraNet® device itself. In addition to RX and TX, there is a TX Enable output for use in multi-drop systems.

Network connection

The CDK provides a single RJ45 Ethernet jack for connection to the CobraNet network. When in use, LEDs on the connector provide status of the network as seen by the CDK-8. The LEDs will be on, off, or flashing depending on the current state of the network connection. Below is a table showing the states of the LEDs and what device status they represent.

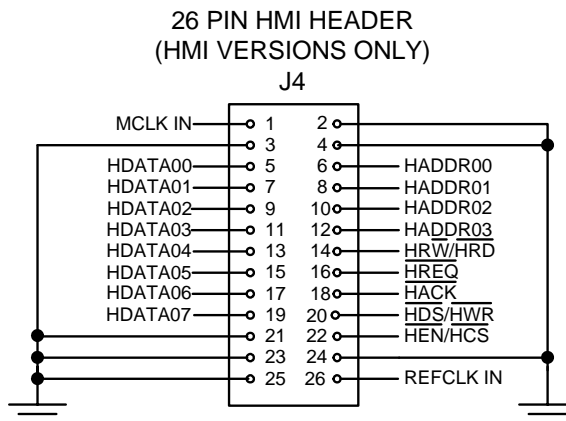
LED status	Device Status
Left LED on permanently. Right LED off	No Ethernet Connection
Left LED on permanently. Right LED on but flashes off every 4 seconds	Ethernet connected but no other CobraNet devices found
Left LED on permanently. Right LED flashing 3 times a second	Connected and CobraNet devices found. Device is a performer.
Left LED on flashing 3 times a second Right LED flashing 3 times a second	Connected and CobraNet devices found. Device is the conductor.

Table 1 - CobraNet Interface LED Status

HMI Port Interfacing (HMI Versions Only)

On CDK-8 modules with HMI support, an additional connector J4 is available to support connection of the Host Management Interface port to a host microcontroller. The 26-way 0.1" female header has all the control signals necessary to implement the HMI interface. It also carries the additional MCLK_IN signal for synchronization with external circuitry.

Pin Descriptions for J1



Pin	Signal	Direction	Notes
2,3,4,21,23,24,25	GND	-	GND
5,7,9,11,13,15,17,19	HDATA00-07	IN/OUT	Host Port Data Port (00-LSB; 07-MSB)
6,8,10,12	HADDR00-03	IN	Host Port Address (00-LSB; 03-MSB)
14	$\overline{\text{HRW}}$ / $\overline{\text{HRD}}$	IN	$\overline{\text{HRW}}$ - Host port transfer direction (Motorola mode) $\overline{\text{HRD}}$ - Host Read (Intel mode)
16	$\overline{\text{HREQ}}$	OUT	Host port data request
18	$\overline{\text{HACK}}$	OUT	Host port interrupt request
20	$\overline{\text{HDS}}$ / $\overline{\text{HWR}}$	IN	$\overline{\text{HDS}}$ - Host port strobe (Motorola mode) $\overline{\text{HWR}}$ - Host write (Intel mode)
22	$\overline{\text{HEN}}$ / $\overline{\text{HCS}}$	IN	$\overline{\text{HEN}}$ - Host port enable (Motorola mode) $\overline{\text{HCS}}$ - Chip select (Intel mode)
1	MCLK IN	IN	For systems featuring multiple CobraNet® interfaces operating off a common master clock.
26	REFCLK IN	IN	Clock input for synchronizing network to an external clock source, for redundancy control and synchronization of FS divider chain to external source.

All logic levels are 3.3 V, but inputs are 5 V tolerant.

Figure 12 - Host Port Read Cycle Timing - Motorola Mode

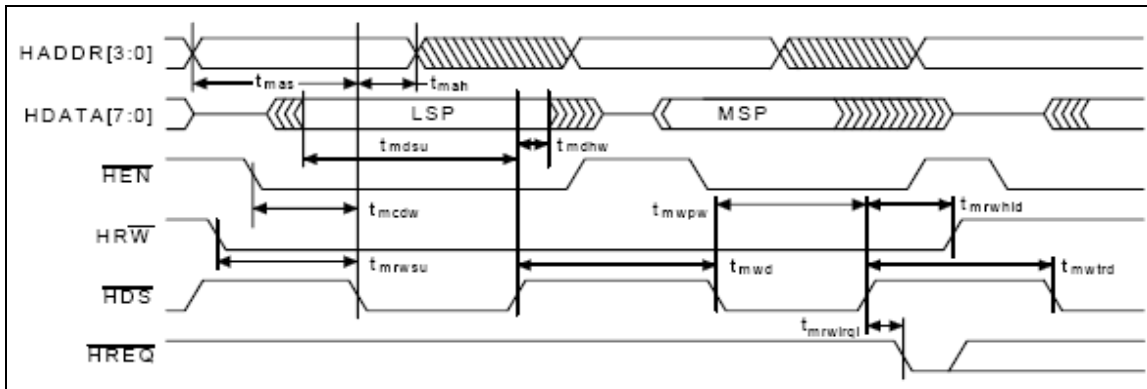


Figure 13 - Host Port Write Cycle Timing - Motorola Mode

Intel Mode

(C_L = 20 pF)

Parameter	Symbol	Min	Max	Unit
Address setup before \overline{HCS} and \overline{HRD} low or \overline{HCS} and \overline{HWR} low	t_{ias}	5	-	ns
Address hold time after \overline{HCS} and \overline{HRD} low or \overline{HCS} and \overline{HWR} high	t_{iah}	5	-	ns
Read				
Delay between \overline{HRD} then \overline{HCS} low or \overline{HCS} then \overline{HRD} low	t_{icdr}	0	-	ns
Data valid after \overline{HCS} and \overline{HRD} low	t_{idd}	-	18	ns
\overline{HCS} and \overline{HRD} low for read	t_{irpw}	24	-	ns
Data hold time after \overline{HCS} or \overline{HRD} high	t_{idhr}	8	-	ns
Data high-Z after \overline{HCS} or \overline{HRD} high	t_{idis}	-	18	ns
\overline{HCS} or \overline{HRD} high to \overline{HCS} and \overline{HRD} low for next read	t_{ird}	30	-	ns
\overline{HCS} or \overline{HRD} high to \overline{HCS} and \overline{HWR} low for next write	t_{irdtw}	30	-	ns
\overline{HRD} rising to \overline{HREQ} rising	$t_{irdirqhl}$	-	12	ns
Write				
Delay between \overline{HWR} then \overline{HCS} low or \overline{HCS} then \overline{HWR} low	t_{icdw}	0	-	ns
Data setup before \overline{HCS} or \overline{HWR} high	t_{idsu}	8	-	ns
\overline{HCS} and \overline{HWR} low for write	t_{iwpw}	24	-	ns
Data hold after \overline{HCS} or \overline{HWR} high	t_{idhw}	8	-	ns
\overline{HCS} or \overline{HWR} high to \overline{HCS} and \overline{HRD} low for next read	t_{iwtrd}	30	-	ns
\overline{HCS} or \overline{HWR} high to \overline{HCS} and \overline{HWR} low for next write	t_{iwd}	30	-	ns
\overline{HWR} rising to \overline{HREQ} falling	$t_{iwrbsyl}$	-	12	ns

NOTES:1. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Hardware handshaking on the \overline{HREQ} pin/bit should be observed to prevent overflowing the input data buffer.

Figure 14 - Host Port Timing Relationships - Intel Mode

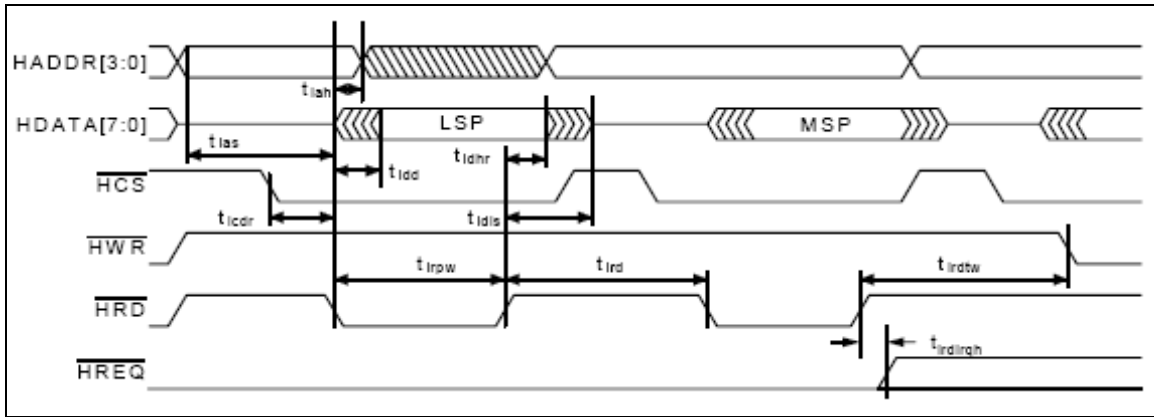


Figure 15 - Host Port Read Cycle Timing - Intel Mode

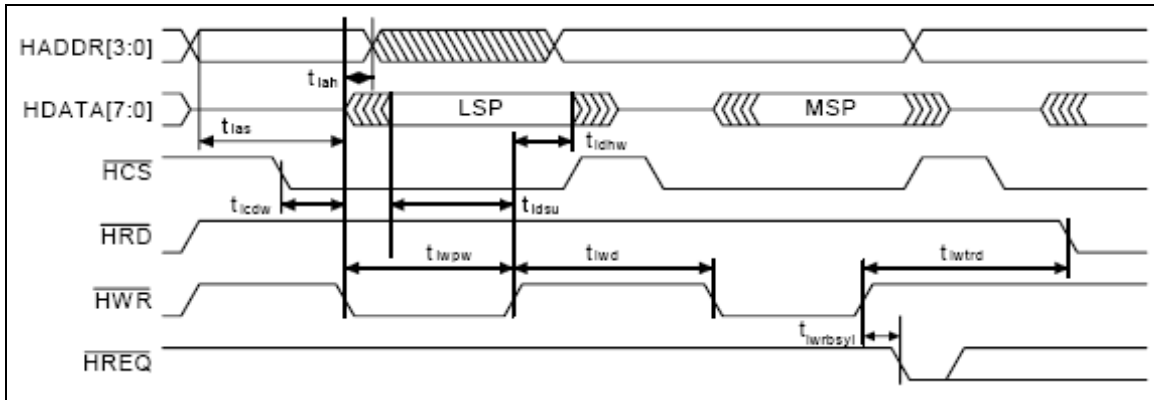
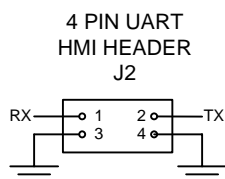


Figure 16 - Host Port Write Cycle Timing - Intel Mode

SHMI Port Interfacing (SHMI Versions only)

On CDK-8 modules with UART HMI support, two additional connectors are available. J2 contains the serial interface connections and J5 has an MCLK_IN connection for synchronization with an external master clock. The serial interface uses TTL level logic so no driver chip is required if it is connected directly to a microcontroller. The pins use 3.3 V logic levels but the inputs are 5 V tolerant.

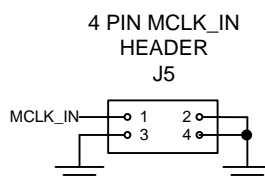
Pin Descriptions for J2 (SHMI Versions Only)



Pin	Signal	Direction	Notes
1	RX	In	HMI UART receive pin
2	TX	Out	HMI UART transmit pin
3,4	GND	GND	GND

Pin Descriptions for J5 (SHMI Versions Only)

This is the second additional connector available on a UART HMI device. This connector is in the same physical location and uses the same connections on the UART board as pins 1 through 4 of J4 on the HMI version of the module.



Pin	Signal	Direction	Notes
1	MCLK IN	IN	For systems featuring multiple CobraNet® interfaces operating off a common master clock.
2,3,4	GND	GND	GND

Interfacing Notes (SHMI Versions Only)

The CDK-8DUART will receive messages from any source capable of communicating serially using 8 data bits, no parity bit, 1 stop bit, and no flow control with a default baud rate of 57600 bits per second (bps). The baud rate is configurable but the data bits, stop bits, flow control, and parity are not.

For details on how to change the UART's baud rate as well as all the details on how to control all the various CobraNet® aspects of the module, see the CDK-8 Design Guide.

Mounting the module

The CDK modules have been designed for easy integration into other products. The only connection required between the CDK-8 and the target hardware is via J1, the mating 26-pin 0.1" header. For CDK-8 modules with the parallel HMI port (J4) or an SHMI port (J2 and J5), the mating connectors must also be available on the target hardware to support use of this feature.

There are three mounting holes available for securing the module, one of which also has a connection to chassis ground. To secure the module to the main board use a 0.1" pitch header (Samtec #MTLW-113-07-G-D-230) and a 0.375in (9.52mm) spacer or pillar.

For details on specific integration recommendations, see the CDK-8 Design guide.

Software Tools

There are a number of CobraNet® software tools available to assist in the development, control and maintenance of CobraNet® enabled products.

Attero Tech Control Center – CobraNet® monitoring and Attero Tech product setup
CobraNet® Discovery – Monitoring and Firmware Updates
CobraCAD – CobraNet® network design tool
DSP Conductor – Drag and Drop user DSP configuration software

Attero Tech Control Center is available on our website, www.atterotech.com. The remaining software is available from Cirrus Logic at <http://www.cobranet.info>.

Firmware Updates

Each CDK-8 is preloaded with a customized version of the most current version of CobraNet® firmware. If a newer version of CobraNet® firmware is released after receiving the CDK-8 module, an update will be made available on the Attero Tech website. If you cannot find the update you require, contact product.support@atterotech.com.

It is important to stress that the initial firmware in the CDK-8 module is a customized version of the CobraNet® base firmware. Be wary of using the latest firmware versions available from the Cirrus website as they will be generic CobraNet® firmware and this will affect the interface between the CDK-8 and the hardware it resides in. The most notable potential problem is the digital audio interface. The generic versions of the CobraNet® firmware set the serial audio format to "Normal" mode where as the CDK-8 uses "I2S" mode in its default configuration.

If any firmware customization is required, contact sales@atterotech.com for more details.

Module Photographs



Figure 17 - CDK-8D

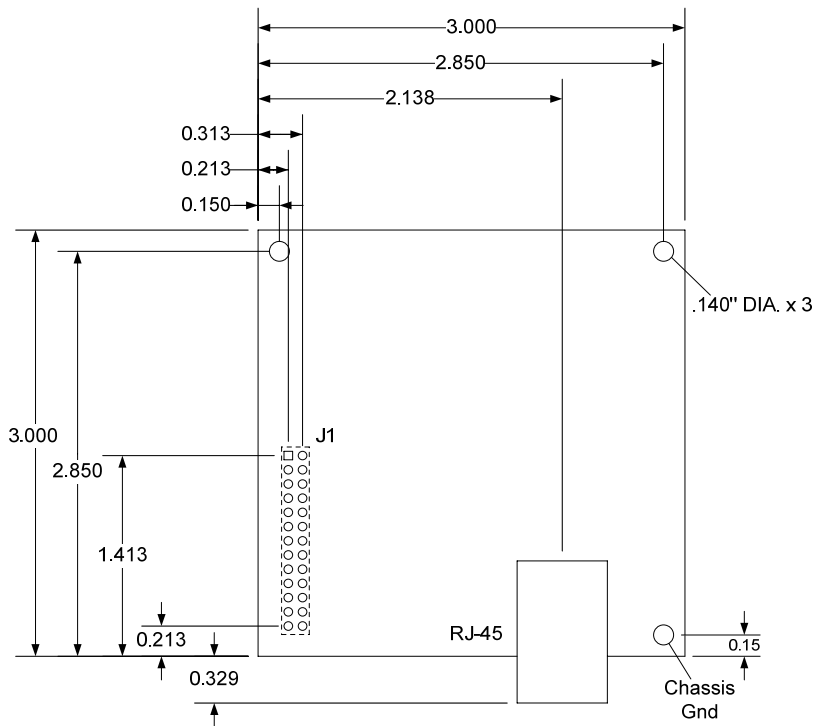


Figure 18 - CDK-8DHMI

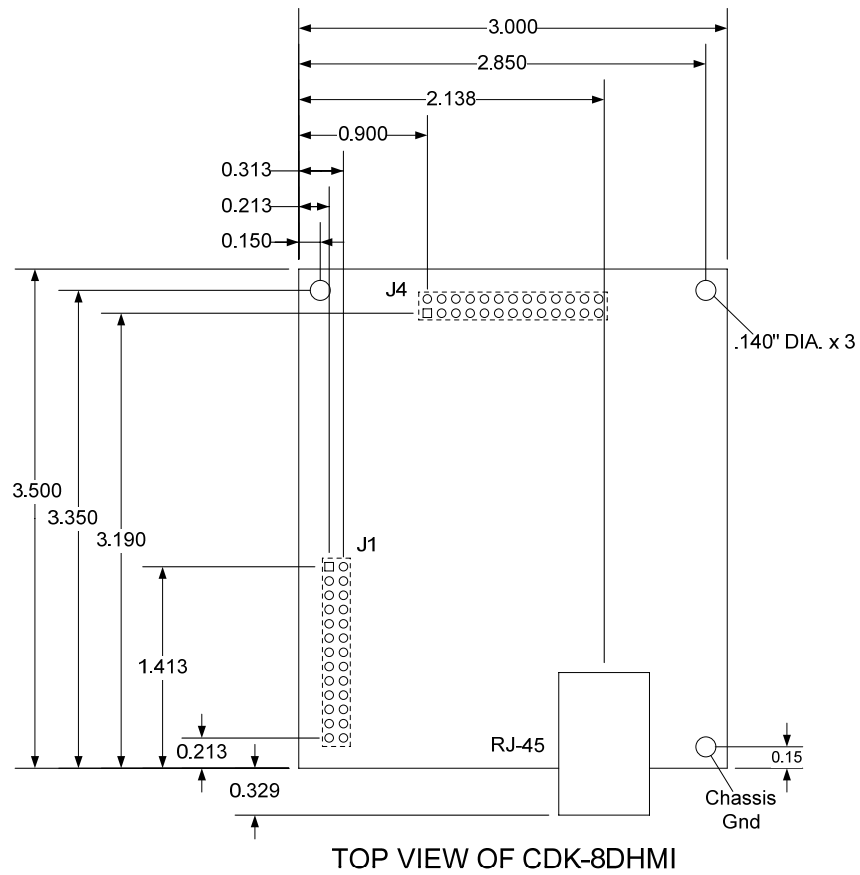


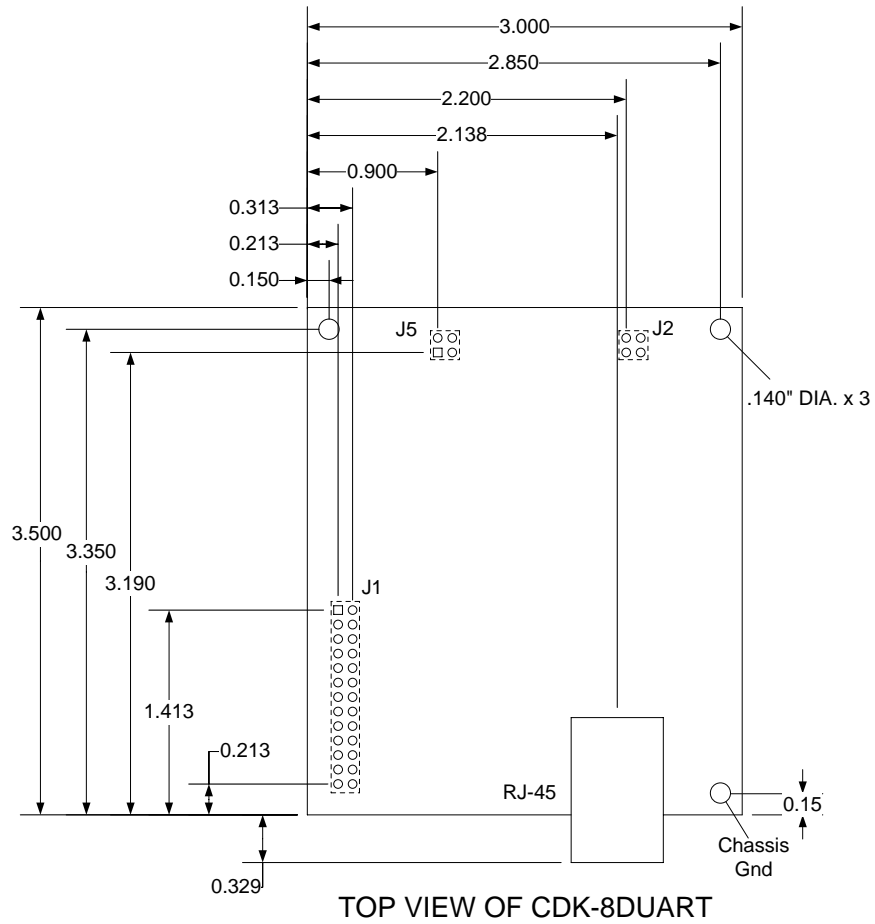
Figure 19 - CDK-8DUART

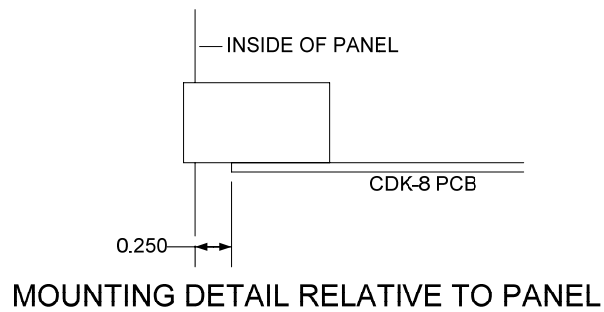
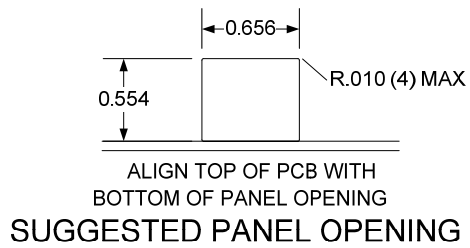
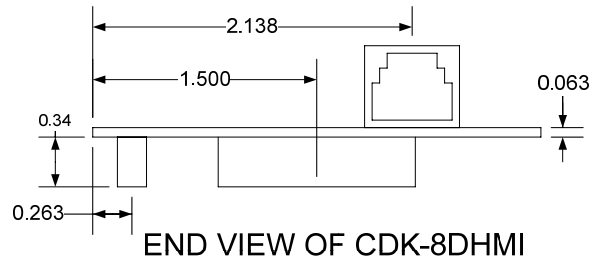
Mechanical Outlines



TOP VIEW OF CDK-8D







Ordering Information

Part Number	Description
CDK-8D	8-channel interface with user DSP
CDK-8DHMI	8-channel interface with parallel HMI port and user DSP
CDK-8DUART	8-channel interface with UART serial HMI port and user DSP